



SMACD 2024
VOLOS - GREECE



2nd – 5th of July, Volos, Greece

SMACD 2024

International Conference on Synthesis, Modeling, Analysis
and Simulation Methods, and Application to Circuit Design

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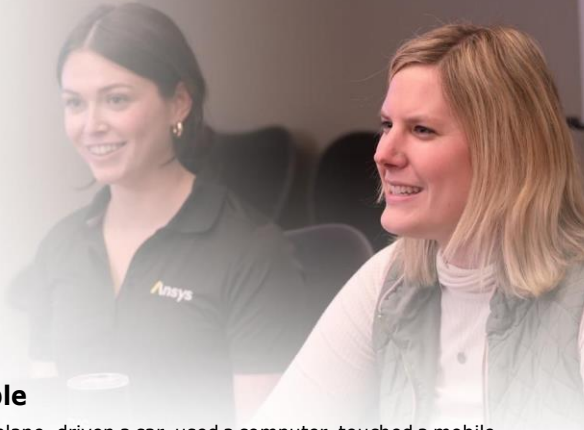
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Tuesday, July 2nd

09:00 - 10:30

Amphitheater 1

Tutorial: "Machine Learning for Design Automation"

11:00 - 12:30

Amphitheater 1

Tutorial: "Tackling Signal Integrity Challenges in Interposer and 3DIC Applications with Ansys RaptorX"

13:30 - 15:00

Amphitheater 1

Tutorial: "Exploring Radiation Effects for Reconfigurable SoCs in Space and Particle Accelerators"

15:30 - 17:00

Amphitheater 1

Tutorial: "Integrating Multiple Knowledge-based Automation Methodologies into the A/MS IC Design Flow"

Wednesday, July 3rd

8:30 - 9:00

Amphitheater 1

Opening Ceremony

9:00 - 10:00

Amphitheater 1

Plenary Talk: *Prof. Yusuf Leblebici*, "Designing Some of the Most Influential Hardware in Human History: Our Collective Responsibilities"

Chair: Alkis Hatzopoulos

1A

10:30 - 12:10

Amphitheater 1

Automated Circuit Design

Chairs: Helmut Graeb, Francisco Fernandez

10:30 Solving the Inverse Problem of Analog Integrated Circuit Sizing with Diffusion Models

Pedro Eid (Instituto de Telecomunicações / Instituto Superior Técnico)

Filipe Azevedo (Instituto de Telecomunicações / Instituto Superior Técnico)

Ricardo Martins (Instituto de Telecomunicações / Instituto Superior Técnico)

Nuno Lourenço (Instituto de Telecomunicações / Instituto Superior Técnico)

10:50 A CAD Toolbox for the Automatic Design and Optimization of ULP CMOS Voltage References

Andrea Boni (University of Parma, Dept. of Engineering and Architecture)

Michele Caselli (University of Parma, Dept. of Engineering and Architecture)

11:10 Advanced Analog Design Optimization: Comparison Between Reinforcement Learning and Heuristic Algorithms

Michel Chevalier (STMICROELECTRONICS)

Severin Trochut (STMicroelectronics)

Roberto Guizzetti (STMicroelectronics)

Pascal Urard (STMicroelectronics)

Lioua Labrak (Institut des Nanotechnologies de Lyon)

Rémy Cellier (Institut des Nanotechnologies de Lyon)

John Samuel (LIRIS)

Nacer Abouchi (Institut des Nanotechnologies de Lyon)

11:30 A novel simulations scheduler for automated circuit sizing algorithms

Catalin Visan (University "Politehnica" of Bucharest)

Dan Curavale (University "Politehnica" of Bucharest)

Georgian Nicolae (University "Politehnica" of Bucharest)

Mihai Boldeanu (University "Politehnica" of Bucharest)

Horia Cucu (University "Politehnica" of Bucharest)

Andi Buzo (Infineon Technologies)

11:50 Algorithm-based Wide-Band Impedance Matching Network Synthesis and Optimization

Anastasios Michailidis (Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki)

Thomas Noulis (Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki)

1B **10:30 - 12:10** **Amphitheater 2**
Special Session: "Advances & Future Trends in Electronic Circuits & Systems with Emerging Devices"
Chairs: Ioannis Messaris, Dimitrios Prousalis

10:30 An Efficient FeFET-Based Compute-In-Memory Macro Readout Inspired by the 3T Pixel Array Cell

Nellie Laleni (*Fraunhofer IPMS*)
Thomas Kämpfe (*Fraunhofer IPMS*)

10:50 Circuit Component Tolerance of Self-Organizing Logic Gates

Haik Manukian (*Naval Information Warfare Center Pacific*)
Osama Nayfeh (*Naval Information Warfare Center Pacific*)
Matthew Kelly (*Naval Information Warfare Center Pacific*)

11:10 Image Processing with Memristor Cellular Nonlinear Networks Featuring Volatile Threshold Switches

Dimitrios Prousalis (*Technische Universität Dresden - TU Dresden*)
Ioannis Messaris (*Technische Universität Dresden*)
Ahmed Ali Sayed (*Technische Universität Dresden*)
Vasileios Ntinis (*Faculty of Electrical and Computer Engineering, Technische Universität Dresden*)
Ahmet Samil Demirkol (*IEE-GE, Technical University of Dresden*)
Alon Ascoli (*Department of Electronics and Telecommunications, Politecnico di Torino*)
Ronald Tetzlaff (*TU Dresden*)

11:30 An Optimization Framework for Mixed-Signal Accelerators Based on F-2T2R Compute Cells

Michele Caselli (*University of Parma*)
Andrea Boni (*University of Parma*)

11:50 FPGA Implementation of an Elementary ReRAM Memory Control Unit

Patricio Carrasco (*Universidad Tecnica Federico Santa Maria*)
Ioannis Vourkas (*Universidad Tecnica Federico Santa Maria*)

13:20 - 13:50
CEDA Presentation

Amphitheater 1

2A **13:50 - 15:30** **Amphitheater 1**
EDA Competition I
Chairs: Elisenda Roca, Vasilis Pavlidis

13:50 Presentation EDA Competition

14:00 Procedural Design, Verification and Implementation Framework for Analog Amplifiers

Veeti Lahtinen (*Department of Electronics and Nanoengineering, Aalto University*)
Santeri Porrasmaa (*Department of Electronics and Nanoengineering, Aalto University*)
Marko Kosunen (*Department of Electronics and Nanoengineering, Aalto University*)
Jussi Rynnänen (*Department of Electronics and Nanoengineering, Aalto University*)

14:30 Automatic Regression Framework for MRAM Compact Models Calibration including Stochasticity

Pierre Graindorge (*imec, University of Liege*)

Bowen Wang (*imec*)

Marie Garcia Bardon (*imec*)

Fernando Garcia Redondo (*imec*)

15:00 Area-Aware Logic Mapping for MAGIC based In-Memory Computing

Jiaxiang Pan (*Ningbo University*)

Zhufei Chu (*Ningbo University*)

2B 13:50 - 15:30 Amphitheater 2
Cutting-edge Technologies for Automotive and Space
Chair: TBD

13:50 Bidirectional CAN-Interface Using Inductive Transmission

Arne von Zedlitz-Neukirch (*Chair of High Frequency Electronics, RWTH Aachen University*)

David Bierbüsse (*Chair of High Frequency Electronics, RWTH Aachen University*)

Renato Negra (*Chair of High Frequency Electronics, RWTH Aachen University*)

14:10 Design and Development of a Linear Adaptive Equalizer used for High Data-Rate Satellite Receivers based on CCSDS 131.2-B Standard

Nico Corsinovi (*University of Pisa*)

Emanuele Pagani (*IngeniArs S.r.l, University of Pisa*)

Roberto Ciardi (*IngeniArs S.r.l, University of Pisa*)

Matteo Bertolucci (*IngeniArs S.r.l.*)

Luca Fanucci (*University of Pisa*)

14:30 Battery Temperature Prediction in Electric Vehicles Using Bayesian Regularization

Rusen Alp Akpınar (*Cranfield University, Faraday Institution and Advanced Propulsion Centre (APC)*)

Abbas Fotouhi (*Cranfield University, Faraday Institution and Advanced Propulsion Centre (APC)*)

Hanwen Zhang (*Cranfield University*)

Daniel Auger (*Cranfield University*)

14:50 The Integration and Testing Procedures for the AcubeSAT Nanosatellite's Software

Antonios Keremidis (*Aristotle University of Thessaloniki*)

Stylios Tzelepis (*National Technical University of Athens*)

Alkis Hatzopoulos (*Electronics Lab, Dept. of Electrical and Computer Eng., Aristotle University of Thessaloniki*)

15:10 Photo Diode Amplifier Design for Radiation Signal Processing with Applications in Mössbauer Spectroscopy for Space Exploration

Mohammad Beyki (*Leibniz University Hannover, Hochschule Hannover - University of Applied Sciences and Arts*)

Justus Pawlak (*Leibniz University Hannover, Hochschule Hannover - University of Applied Sciences and Arts*)

Robert Patzke (*Hochschule Hannover - University of Applied Sciences and Arts*)

Franz Renz (*Institute of Inorganic Chemistry, Leibniz University, Hannover, D-30167, Germany*)

3A

16:00 - 17:00

Amphitheater 1

Innovations in Hardware Security I

Chair: Giulia di Capua

16:00 Harvesting RTN for True Random Number Generators and Physical Unclonable FunctionsFrancisco J. Rubio Barbero (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Fernando de Los Santos Prieto (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Rafael Castro Lopez (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Elisenda Roca Moreno (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Francisco V. Fernandez Fernandez (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)**16:20 Proposal and Implementation on Smartphone of a PUF Using Accelerometers and Gyroscopes**Raúl Aparicio-Téllez (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Miguel Garcia-Bosque (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Guillermo Diez-Senorans (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Abel Naya (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Santiago Celma (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)**16:40 Sensitivity-aware Hardware Trojan Injection for SET Propagation and Soft Error Attacks**Alexandra Takou (*University of Thessaly*)Georgios-Ioannis Paliaroutis (*University of Thessaly*)Pelopidas Tsoumanis (*University of Thessaly*)George Stamoulis (*University of Thessaly*)Nestor Evmorfopoulos (*University of Thessaly*)

3B

16:00 - 17:00

Amphitheater 2

Machine Learning for Modeling

Chair: Alex Doholi

16:00 Neural Network-Based Coefficient Estimators for Memory Polynomial Digital PredistortionElif Seher Serinken (*Yildiz Technical University Electronics and Communications Engineering Department*)Alperen Tunç (*Istanbul Technical University Electronics and Communications Engineering Department*)Revna Acar-Vural (*Yildiz Technical University Electronics and Communications Engineering Department*)Mustafa Berke Yelten (*Istanbul Technical University Electronics and Communications*)**16:20 Low-Power 9.6-11GHz and 10.8-12GHz VCOs Designed for a 2.5/5GHz TRx using High-Q Inductors Synthesized with ML Techniques**Fabio Passos (*Instituto de Telecomunicações*)Nuno Lourenço (*Instituto de Telecomunicações*)Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon*)**16:40 An Open-Source ANN-based Analog/RF Intellectual Property for SkyWater130nm Technology**Enes Sağlıcan (*Gebze Technical University*)Engin Afacan (*Gebze Technical University*)

Thursday, July 4th

8:30 - 9:30

Amphitheater 1

Plenary Talk: *Prof. Georges Gielen*, "Designing Analog Integrated Circuits: Designers, Synthesis or Generative AI?"

Chair: Francisco Fernandez

4A

9:30 - 10:30

Amphitheater 1

EDA Competition II

Chairs: Elisenda Roca, Vasilis Pavlidis

9:30 **Multiple Output Modelling of Integrated Circuits Behavior Using an Active Learning Approach**

Vasile Grosu (*"Gheorghe Asachi" Technical University of Iasi*)

David Emilian (*Infineon Technologies*)

Liviu Goras (*"Gheorghe Asachi" Technical University Iasi*)

Georg Pelz (*Infineon Technologies AG Neubiberg*)

10:00 **Fast ML-driven Analog Circuit Layout using Reinforcement Learning and Steiner Trees**

Davide Basso (*University of Trieste*)

Luca Bortolussi (*University of Trieste*)

Mirjana Videnovic-Misic (*Infineon Technologies Austria*)

Husni Habal (*Infineon*)

11:00 - 12:00

Amphitheater 1

Sponsor Presentations

5A

13:40 - 15:00

Amphitheater 1

Automating Layout and Technology Migration

Chair: Jürgen Scheible

13:40 **Effective Routing Probability Maps via Convolutional Neural Networks for Analog IC Layout Automation**

Diogo Penada (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

Nuno Lourenço (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

Nuno Horta (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

14:00 Mitigating Power and Process Variation for Analog CIM Design Migration

Shih-Han Chang (*National Yang Ming Chiao Tung University*)
Shih-Yu Chen (*National Yang Ming Chiao Tung University*)
Chun-Wen Yang (*National Yang Ming Chiao Tung University*)
Hau-Wei Huang (*National Yang Ming Chiao Tung University*)
Yu-Cheng Yang (*National Yang Ming Chiao Tung University*)
Wei-Liang Chen (*National Yang Ming Chiao Tung University*)
Chien-Nan Liu (*National Yang Ming Chiao Tung University*)
Hung-Ming Chen (*National Yang Ming Chiao Tung University*)

14:20 Ternary Clock Tree Synthesis for 3D ICs

Christos Pavlidis (*Aristotle University of Thessaloniki*)
Nikos Sketopoulos (*University of Thessaly*)
Christos Sotiriou (*University of Thessaly*)
Vasilis Pavlidis (*Aristotle University of Thessaloniki*)

14:40 PONDEROUS: A Performance-driven Analog IC Placement Optimizer Leveraged by a ML Pipeline

Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)
António Gusmão (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)
Rafael Vieira (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)
Fábio Passos (*Instituto de Telecomunicações, Portugal*)
Nuno Lourenço (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)
Nuno Horta (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

5B**13:40 - 15:00****Amphitheater 2****Advanced Circuit Design I****Chair: Ioannis Vourkas****13:40 Carry-chain based Ring Oscillator Design for Temperature Sensing on FPGAs**

Fanny Spagnolo (*University of Calabria - DIMES*)
Pasquale Corsonello (*University of Calabria - DIMES*)

14:00 A Hardware Efficient Digital DAC Linearization Topology for Delta-Sigma ADCs

Jesko Flemming (*Institute for Sensors and Automation, University of Applied Sciences and Arts Hannover, Germany*)
Timon Rogge (*Institute for Sensors and Automation, University of Applied Sciences and Arts Hannover, Germany*)
Bernhard Wicht (*Institute of Microelectronic Systems, Leibniz University Hannover*)
Pascal Witte (*Institute for Sensors and Automation, University of Applied Sciences and Arts Hannover, Germany*)

14:20 A PWM-SAR ADC with Asynchronous Control Unit for Mixed-Signal Accelerators

Michele Caselli (*University of Parma*)
Andrea Boni (*University of Parma*)
Stefano Caselli (*University of Parma*)

14:40 3.35V High Voltage Electroforming Generator in 28nm with 5.3mV ripple and 46% efficiency for HfO₂ based Memristors

Muhammad Shamookh (*Forschungszentrum Jülich-ZEA-2, IIC Technische Universität Hamburg*)
Arun Ashok (*Forschungszentrum Jülich-ZEA-2*)
Andre Zambanini (*Forschungszentrum Jülich-ZEA-2*)

6A

15:30 - 16:30

Amphitheater 1

EDA and the Human Factor

Chair: Engin Afacan

15:30 Streamlined design methodology for Cell-Based DCOsAndres Santana-Andreo (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)J.M. Gata-Romero (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)Rafael Castro-Lopez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)Elisenda Roca (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)Francisco Vidal Fernandez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)**15:50 Design of a Two-Stage Miller-Compensated Operational Amplifier Using a Designer-in-the-Loop EDA Approach**Yijia Hao (*University of Glasgow*)Miguel Gandara (*Mediatek Inc.*)Srinjoy Mitra (*University of Edinburgh*)Sandy Cochran (*University of Glasgow*)Bo Liu (*University of Glasgow*)**16:10 Automatically Understanding Human Behavior for IoT Applications with Optimized Human-in-the-Loop Control**Himavanth Reddy Pallapu (*Stony Brook University, Department of ECE*)Gnaneswar Villuri (*Stony Brook University, Department of ECE*)Simona Doboli (*Department of Computer Science*)Alex Doboli (*Stony Brook University, Department of ECE*)

6B

15:30 - 16:30

Amphitheater 2

Special Session: "Safety and Security in System-on-Chip (SoC)"

Chair: Eleonora Vacca

15:30 OP-TEE powered OpenSSL Engine enhancing Digital Signature security for ARM ArchitecturesFranco Volante (*Politecnico di Torino*)Francesco Barchi (*Università di Bologna*)Edoardo Patti (*Politecnico di Torino*)Lorenzo Bottaccioli (*Politecnico di Torino*)Luca Barbierato (*Politecnico di Torino*)**15:50 Exploring the Resiliency of Hardware CNN for Aerospace Application**Corrado De Sio (*Politecnico di Torino*)Giorgio Cora (*Politecnico di Torino*)Sarah Azimi (*Politecnico di Torino*)Eleonora Vacca (*Politecnico di Torino*)Luca Sterpone (*Politecnico di Torino*)**16:10 End-to-end Integration of OpenTitan Security Features in a Pure RISC-V SoC**Alberto Musa (*Università di Bologna*)Emanuele Parisi (*Università di Bologna*)Luca Barbierato (*Politecnico di Torino*)Andrea Acquaviva (*Università di Bologna*)Francesco Barchi (*Università di Bologna*)

Friday, July 5th

7A

9:30 - 10:30

Amphitheater 1

Novel Device Modeling and Characterization

Chair: *TBD*

9:30 Method, Testing Procedure and System for the Experimental Characterization of Power Inductors

Giulia Di Capua (University of Cassino and Southern Lazio)
Nicola Femia (DIEM - University of Salerno)
Nunzio Oliva (Exeling Srl)
Luca De Guglielmo (Exeling Srl)

9:50 A Verilog-A/MS Compact Model for the Temperature Dependency of the Open-Circuit Voltage for Integrated Diodes

Pablo Fernández-Peramo (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)
Juan Antonio Leñero-Bardallo (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)
Sergio Palomeque-Mangut (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)
Ángel Rodríguez-Vázquez (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)

10:10 Towards a Digital Twin of a Time-Dependent Variability Characterization Laboratory

J.M. Gata-Romero (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)
E. Roca (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)
R. Castro-Lopez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)
F.V. Fernandez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)

7B

9:30 - 10:30

Amphitheater 2

Advanced circuit design II

Chair: *Michele Caselli*

9:30 A New Metric Measuring Steering Accuracy of Digitally Controlled Phase Shifters

Francisco Aznar (*Centro Universitario de la Defensa Zaragoza*)
Uxua Esteban-Eraso (*Universidad de Zaragoza*)
Antonio Dionisio Martínez-Pérez (*Universidad de Zaragoza*)
Santiago Celma (*Universidad de Zaragoza*)

9:50 A 25 nW Heartbeat Monitoring Circuit for Wearable Applications in CMOS 65nm

Rafael Vieira (*Instituto de Telecomunicações*)
Seyedehsomayeh Hatefinasab (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon*)
Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon*)
Nuno Horta (*Instituto de Telecomunicações*)

10:10 Low-Power Encoding for PAM-3 DRAM Bus

Jonghyeon Nam (*Hanyang University*)
Jaeduk Han (*Hanyang University*)
Hokeun Kim (*Arizona State University*)

8A

11:00 - 12:40

Amphitheater 1

Machine Learning for Design

Chair: TBD

11:00 A learning-based method for performance optimization of timing analysis

Anastasis Vagenas (*University of Thessaly*)
Dimitrios Garyfallou (*University of Thessaly*)
Nestor Evmorfopoulos (*University of Thessaly*)
George Stamoulis (*University of Thessaly*)

11:20 Optimizer-Free Sizing of OpAmps Leveraging Structural and Functional Properties

Markus Leibl (*Technical University of Munich (TUM)*)
Helmut Graeb (*Technical University of Munich (TUM)*)

11:40 Frontend-Backend Integrated Circuit Device Linking Using Machine Learning Algorithms

Ingrid Kovacs (*Technical University of Cluj-Napoca*)
Bianca Carbunescu-Stoenescu (*Technical University of Cluj-Napoca*)
Andi Buzo (*Infineon Technologies AG Neubiberg*)
Emilian David (*Infineon Technologies Bucharest*)
Georg Pelz (*Infineon Technologies AG Neubiberg*)
Marina Topa (*Technical University of Cluj-Napoca*)

12:00 ANN-based Analog/RF IC Synthesis Featuring Reinforcement Learning-based Fine-Tuning

Hakan Taşkıran (*Gebze Technical University*)
Enes Sağlıcan (*Gebze Technical University*)
Engin Afacan (*Gebze Technical University*)

12:20 Analog Circuit Classification Using Graph Convolution Networks

Husni Habal (*Infineon Technologies AG*)
Marco De Maina (*Infineon Technologies AG*)
Vishnu Pathak (*Infineon Technologies India Pvt. Ltd.*)
Karthik Salian (*Infineon Technologies India Pvt. Ltd.*)

8B

11:00 - 12:40

Amphitheater 2

IC Design Contest

Chairs: Georgios Panagopoulos, Dimitrios Garyfallou

11:00 Set the Clock: A Synthesizable Clock Manager

Jonas Lienke (*Insitut für Mikroelektronik und Mechatronik Systeme gemeinnützige GmbH*)
Florian Kögler (*IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH*)
Eric Schäfer (*IMMS GmbH*)
Georg Gläser (*Insitut für Mikroelektronik und Mechatronik Systeme gemeinnützige GmbH*)

11:25 Two Stage Diode-String Architecture for Ultra-Low Power Digital to Analog Converters

Andreas Tsioungkos (*Aristotle University of Thessaloniki*)
Moschos Antoniadis (*Aristotle University of Thessaloniki*)
Vasilis Pavlidis (*Aristotle University of Thessaloniki*)

11:50 Rapid Prototyping Platform for Integrated Circuits for Quantum Computing

Jonas Mair (ZEA-2)

Sabitha Kusuma (ZEA-2)

Daniel Liebau (ZEA-2)

Lammert Duipmans (ZEA-2)

Patrick Vliex (ZEA-2)

André Zambanini (ZEA-2)

Stefan van Waasen (ZEA-2, *Uni DUE*)

12:15 DTCO for Fast STT-MRAM Periphery Operation

Ahmed Hossam-Eldeen (IMEC, Leuven, Belgium / University of Gent, Gent, Belgium)

Bowen Wang (IMEC, Leuven, Belgium), Priyanka Pandey (IMEC, Leuven, Belgium)

Marie Garcia Bardon (IMEC, Leuven, Belgium)

Fernando Garcia Redondo (IMEC, Leuven, Belgium)

9A**13:50 - 14:50****Amphitheater 1****Advanced Circuit Modeling****Chair: Nicola Femia****13:50 Efficient Parametric Model Order Reduction for Large-Scale Circuit Models using Extended Krylov Subspace**

Chrysostomos Chatzigeorgiou (University of Thessaly)

George Floros (University of Thessaly)

Dimitrios Chatzigeorgiou (University of Thessaly)

Nestor Evmorfopoulos (University of Thessaly)

George Stamoulis (University of Thessaly)

14:10 Propagation Delay Estimation for Mixed-Signal Modeling of Comparators

Martin Grabmann (IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH))

Eric Schäfer (IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH))

Georg Gläser (IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH))

14:30 Analysis and Simulation of Reset Leakage Currents and Quantization Error in a PFM Digital Pixel

Sergio Palomeque-Mangut (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

Pablo Fernández-Peramo (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

Juan Antonio Leñero-Bardallo (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

Ángel Rodríguez-Vázquez (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

9B**13:50 - 14:50****Amphitheater 2****Innovations in Hardware Security II****Chair: Ricardo Martins****13:50 Optimization-based bit selection technique to improve the reliability of PUFs**

Fernando de Los Santos Prieto (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Francisco Javier Rubio Barbero (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Rafael Castro López (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Elisenda Roca Moreno (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Francisco V. Fernández Fernández (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

14:10 Towards the Implementation of a Strong PUF using Generalized Galois Ring Oscillators

Raúl Aparicio-Téllez (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

Miguel Garcia-Bosque (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

Guillermo Diez-Senorans (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

Santiago Celma (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

14:30 A Fast Security Closure Approach for EM-based Attacks on General Multi-Segment Interconnects

Pavlos Stoikos (*University of Thessaly*)

George Floros (*University of Thessaly*)

Nestor Evmorfopoulos (*University of Thessaly*)

George Stamoulis (*University of Thessaly*)

10A

15:20 - 16:20

Amphitheater 1

Dealing with Reliability

Chair: Alkiviadis Hatzopoulos

15:20 Stress-based Electromigration Modeling in IC Design: Moving from Theory to Practice

Susann Rothe (*Dresden University of Technology*)

Jens Lienig (*Dresden University of Technology*)

Sachin S. Sapatnekar (*University of Minnesota*)

15:40 An Efficient Approach for Combined Electromigration and Thermomigration Analysis Based on the Extended Krylov Subspace

Eleni Tselepi (*University of Thessaly*)

Olympia Axelou (*University of Thessaly*)

George Floros (*University of Thessaly*)

George Stamoulis (*University of Thessaly*)

16:00 Analysis of Capacitive Coupling and Crosstalk in the PCB of Switch-Mode Power Supplies

Giulia Di Capua (*University of Cassino and Southern Lazio*)

Antonio Maffucci (*University of Cassino and Southern Lazio*)

Nicola Femia (*University of Salerno*)

Andrea Gaetano Chiariello (*Università degli Studi della Campania "Luigi Vanvitelli"*)

10B

15:20 - 16:20

Amphitheater 2

Dealing with Verification

Chair: Miguel Garcia Bosque

15:20 Efficient Stimuli Generation using Reinforcement Learning in Design Verification

Deepak Narayan Gadde (*Infineon Technologies Dresden GmbH & Co. KG*)

Thomas Nalapat (*Infineon Technologies Dresden GmbH & Co. KG*)

Aman Kumar (*Infineon Technologies Dresden GmbH & Co. KG*)

Sebastian Simon (*Infineon Technologies Dresden GmbH & Co. KG*)

Djones Lettnin (*Infineon Technologies AG*)

15:40 Formal Verification of Nonlinear Analog Circuits using State Space-Based Model Order Reduction

Yasmine Abu-Haeyeh (*University of Frankfurt*)

Lars Hedrich (*University of Frankfurt*)

16:00 Low-rank balanced truncation of RLCK models via frequency-aware rational Krylov-based projection

Christos Giamouzis (*University of Thessaly*)

Dimitrios Garyfallou (*University of Thessaly*)

Nestor Evmorfopoulos (*University of Thessaly*)

16:20 - 16:50

Amphitheater 1

Award Ceremony and Closing