



SMACD 2024  
VOLOS - GREECE



2<sup>nd</sup> – 5<sup>th</sup> of July, Volos, Greece

# SMACD 2024

International Conference on Synthesis, Modeling, Analysis  
and Simulation Methods, and Application to Circuit Design

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## For more information please contact:

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Wednesday, July 3<sup>rd</sup>, 9:00 – 10:00

## “Designing Some of the Most Influential Hardware in Human History: Our Collective Responsibilities”

Prof. Yusuf Leblebici

*Sabanci University, Turkey*

### Abstract

As circuit and system designers, we have been responsible for bringing to life some of the most ubiquitous hardware during the last 50 years, including microprocessors, memory chips, wireless and wireline communication circuits, and data converters – all of which have profoundly influenced how we perceive our world, and how we interact with other human beings. Now, two very powerful technologies, namely AI/ML and quantum sensing/computing, are converging to change the human experience fundamentally, mainly thanks to the hardware infrastructure, designed by us, that enables them. In the case of AI, the influence flows both ways: While the capabilities of ever more powerful AI platforms are enabled by the hardware infrastructure, the availability of AI-enabled tools will also enhance the capabilities of the new hardware that is designed by using AI. The enormous potential of quantum computing, on the other hand, will likely influence fundamental changes in our thinking, and in our perception of “reality”. As designers of the hardware platforms that enable these revolutions, it is incumbent upon us to be aware of our responsibilities and to act accordingly.



**Yusuf Leblebici** received the BSc and MSc degrees in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 1984 and 1986, respectively, and the PhD degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign (UIUC), IL, USA, in 1990. In 2002, he was appointed as a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL) and Director of the Microelectronic Systems Laboratory which he led for more than 16 years. In November 2018, he was appointed as President of Sabancı University. His research

interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. So far, he has graduated 58 PhD students and

more than 100 MSc students. He is the coauthor of nine books (including two internationally acclaimed textbooks), as well as more than 350 scientific articles published in various journals and conferences.

Yusuf Leblebici has been the recipient of the prestigious Young Scientist Award of the Turkish Scientific and Technological Research Council in 1995, and the "Joseph S. Satin Distinguished Fellow Award" in 1999. He was elected as an IEEE Fellow in 2009, and as a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011. In 2020, Yusuf Leblebici has received the Electrical and Computer Engineering Distinguished Alumni Award from the University of Illinois at Urbana-Champaign (UIUC), and in 2023, he was elected as a Member of Academia Europaea.

Thursday, July 4<sup>th</sup>, 8:30 – 9:30

## “Designing Analog Integrated Circuits: Designers, Synthesis or Generative AI?”

Prof. Georges Gielen

*KU Leuven, Belgium*

### Abstract

Analog/mixed-signal integrated circuits are key in applications where electronics interface with the physical world. But whereas digital circuits are largely synthesized through EDA software, surprisingly, the design of analog circuits in industry is mainly still handcrafted, resulting in long and error-prone design cycles and high development costs. The rebirth of AI and machine learning, and the recent rise of generative AI (GenAI) methods, however, create a whole new spectrum of techniques to automate this process. This keynote will explore the high potential of using advanced machine learning (ML) techniques to automatically synthesize and lay out analog circuits, even to create new circuit structures. What will be feasible? Will we still need designers?.



**Georges G.E. Gielen** received the MSc and PhD degrees in Electrical Engineering from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1986 and 1990, respectively. Currently, he is Full Professor in the MICAS research division at the Department of Electrical Engineering (ESAT) at KU Leuven. From August 2013 until July 2017 he served as Vice-Rector for the Group of Sciences, Engineering and Technology. He was visiting professor at UC Berkeley and Stanford University. Since 2020 he is Chair of the Department of Electrical Engineering (ESAT) at KU Leuven.

His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation, including modeling, simulation, optimization and synthesis as well as testing. He is a frequently invited speaker/lecturer and coordinator/partner of several (industrial) research projects in this area, including an ERC Advanced Grant. He has (co-)authored 10 books and more than 700 publications in edited books, international journals and conference proceedings. He is a 1997 Laureate of the Belgian Royal Academy of Sciences, Literature and Arts in the discipline of Engineering. He is Fellow of the IEEE since 2002, and received the IEEE CAS Mac Van Valkenburg award in 2015 and the IEEE CAS Charles Desoer award in 2020, as well as the EDAA Achievement Award in 2021. He is an elected member of the Royal Flemish Academy of Belgium in the class of Technical Sciences, and of the Academia Europaea.

Tuesday, July 2<sup>nd</sup>, 09:00 – 10:30

## “Machine Learning for Design Automation”

The widespread usage of machine learning and deep learning has fundamentally reshaped the information infrastructure and human society. It also brings new opportunities for design automation of VLSI. With machine learning techniques, labor intensive and time-consuming IC design cycles can be accelerated effectively. This tutorial will present recent research progress on machine learning for various stage in design automation, especially on high level synthesis, timing analysis, thermal modeling and yield analysis.

### Talk 1: Heuristic Method for High-level Synthesis

**Prof. Kang Zhao**, Beijing University of Telecommunications, Beijing China

With the increasing speed of chip design iteration, high-level synthesis (HLS) technology is considered an effective shortcut to achieve agile design and development. HLS mainly automatically converts C/C++-high-level descriptions into appropriate hardware RTL descriptions, and performs prototype verification on FPGA. The report will introduce high-level integrated processes and key compilation scheduling techniques. From the perspective of the academic community, analyze the difficulties and challenges which can be solved using heuristic algorithms.

### Talk 2: Machine Learning for Thermal Modeling and Timing

**Prof. Yuanqing Cheng**, Beihang University, Beijing, China

As the integration density on-chip increases quickly with technology node shrinking, thermal dissipation becomes a severe problem for high performance chip design. Although traditional analytical models can capture on-chip thermal profile accurately, they are usually very time-consuming, and difficult to be integrated with iterative physical design phase. So in the first part of this talk, I will introduce recent research progress on using machine learning for thermal modeling such that the thermal aware physical design can be effectively accelerated and the hotspot can be captured as early as possible to mitigate thermal issues before sign-off stage. In addition, today's billion scale chip design makes timing closure a challenging task due to sharply increase of process corners. In the second part of this talk, I will present how to take advantage of machine learning to accelerate timing analysis for deep sub-micron VLSI design.

# Talk 3: AI Powered Sampling Methods for Yield Analysis and Optimization

**Prof. Wei W. Xing**, Sheffield University, Sheffield, UK

Yield estimation and optimization are two fundamental problems in back end electronic design automation (EDA), particular with the latest technology nodes. In this tutorial, we will introduce how the latest AI method can boost up the yield analysis and optimization with significant speedup and accuracy improvement. From the perspective of the academic community, outline the difficulties and challenges which can be solved using modern AI methods.

**Tuesday, July 2<sup>nd</sup>, 11:00 – 12:30**

## “Tackling Signal Integrity Challenges in Interposer and 3DIC Applications with Ansys RaptorX”

**Georgia Krokou**, ANSYS, GR

In the evolving landscape of heterogeneous integration, designers face multiphysics challenges in ensuring signal integrity on silicon interposers and 3DIC architectures. Co-extraction of the signals with the power and ground nets to account for all potential electromagnetic coupling is crucial. Ansys RaptorX offers a robust solution, ensuring secure and efficient sign-off by addressing these signal integrity challenges with its advanced modeling capabilities. In this tutorial, case studies will be presented to showcase the strength of the RaptorX modeling engine, followed by a live demonstration of the tool on an interposer design.

**Tuesday, July 2<sup>nd</sup>, 13:30 – 15:00**

## **“Exploring Radiation Effects for Reconfigurable SoCs in Space and Particle Accelerators”**

The tutorial provides an in-depth overview of electronic failures induced by radiation in radioactive environments, such as space and particle accelerators. The first part delves into the radiation effects, considering the radiation environment of the Large Hadron Collider (LHC) at CERN, emphasizing comparisons with atmospheric conditions. The second part focuses on the reliability analysis of Reconfigurable Systems-on-Chip, discussing challenges and methodologies for evaluating radiation-induced effects on these systems.

### **Talk 1: Electronic Failures in the Accelerator Radiation Environment and Test Facilities**

**Dr. Matteo Cecchetto**, CERN

The talk introduces the radiation-induced effects in electronics, with a particular focus on the radiation environment in the Large Hadron Collider (LHC) accelerator at CERN, presenting several comparisons with the atmospheric environment. It shows how the radiation levels are measured and simulated in critical areas of the accelerator, focusing on thermal and higher energy neutrons, which are one of the main threats for SEEs. Indeed, SEEs induced by thermal, and 0.01-10 MeV neutrons can induce more failures than high energy neutrons in several locations of the accelerator, and the related Radiation hardness Assurance (RHA) implications are presented. Finally, an overview of the test facilities employed at CERN to measure and qualify electronics is outlined.

### **Talk 2: Reliability Analysis for Reconfigurable Systems-on-Chip**

**Dr. Corrado De Sio**, Politecnico di Torino

Thanks to their performance, reduced power consumption, and adaptability, Reconfigurable Systems-on-Chip has emerged as a cutting-edge platform for many performance-oriented applications. Additional efforts are needed to ensure the correct system functionality for applications where reliability is a primary concern. Radiation environments are particularly challenging due to the high sensitivity of SRAM-based reconfigurable systems to single-event effects. The tutorial focuses on motivation, challenges, and methodology for evaluating radiation-induced effects on Reconfigurable Systems-on-Chip.

**Tuesday, July 2<sup>nd</sup>, 15:30 – 17:00**

## **“Integrating Multiple Knowledge-based Automation Methodologies into the A/MS IC Design Flow”**

In the rapidly evolving field of integrated circuit (IC) design, the quest for efficiency, miniaturization, and power optimization has led to the development of innovative methodologies that promise to redefine traditional design flows. This tutorial presents a holistic approach to analog/mixed-signal IC design, focusing on the integration of cutting-edge techniques such as the gm/ID method for transistor sizing, Expert Design Plan (EDP) for procedural design automation in combination with ML characterization, Intelligent IP (IIP) for technology-agnostic schematic and layout generation, and SWARM for autonomous layout optimization. Aimed at both industry professionals and academic researchers, this tutorial will provide a deep dive into each method, showcasing how they can be synergistically applied in the future to streamline the design process, enhance design quality, and accelerate the development of ultra-low power (ULP) sensors and analog/mixed-signal (A/MS) circuits.

### **Talk 1: gm/ID and Machine Learning Sizing**

**Prof. Ralf Sommer**, TU Ilmenau, DE

**Lorenz Renner**, TU Ilmenau, DE

**Yannick Uhlmann**, Reutlingen University, DE

The presentation introduces the gm/ID method, an advanced technique for efficiently sizing transistors based on their operating points. Unlike traditional approaches such as the Square-Law method, the gm/ID method utilizes characteristic curves or lookup tables derived from a multidimensional DC analysis of the SPICE transistor model. This allows for accurate transistor sizing without the need for post-simulation adjustments, as the sizes are directly derived from the characteristic curves.

The second part focuses on the innovative use of neural networks (NNs) for transistor sizing using the gm/ID method. Neural networks learn from existing lookup tables and capture complex relationships to enhance accuracy without requiring extensive storage. This technique allows design strategies to be expressed in terms of electrical characteristics, reducing dependence on geometric quantities and process design kits (PDKs) and enabling efficient sampling and characterization of entire circuits.

## Talk 2: EDP for Circuit Design

**Prof. Jürgen Scheible**, Reutlingen University, DE

In the second block of the tutorial, the Expert Design Plan (EDP) is discussed. EDP is an approach that encapsulates the knowledge and methodology of experienced analog designers in a reusable script. EDP enables designers to automate the entire design process from topology creation to final sizing using a special language (EDPL) and a comprehensive toolset. This includes functions for drawing circuit diagrams, setting up and executing simulations, evaluating simulation results, and exploring the design space. Previous EDP applications show that a bandgap reference circuit can be designed in less than 15 minutes and the analog parts of a 10-bit SAR-ADC fully automatically in about 100 minutes. In the talk the user interface and usage of EDP for a simple design task is demonstrated.

## Talk 3: Layout: SWARM & Intelligent IP

**Dr. Benjamin Prautsch**, Fraunhofer IIS/EAS

**Till Moldenhauer**, Reutlingen University, DE

The third part of the tutorial focuses on innovative A/MS layout methodologies. The two specific methods SWARM and Intelligent IP (IIP) will be presented. SWARM uses a decentralized approach with both formalized and non-formalized knowledge where self-organizing modules autonomously develop an optimal layout for given constraints. This method leads to compact and efficient chip layouts. IIP employs generator-based and template-based methods such that it enables technology-independent description and automation of schematics and layouts. It facilitates the transfer of designs between different manufacturing processes while preserving design integrity. The talks emphasize the advantages of these methods in terms of layout creation speed, high usability with low initial efforts, as well as flow integration that will help design engineers in product development.

Wednesday, July 3<sup>rd</sup>, 10:30 – 12:10

Amphitheater 2

## Advances & Future Trends in Electronic Circuits & Systems with Emerging Devices

The field of electronic circuits and systems is at a crossroads, prepared to leverage the transformative capabilities of emerging devices that are expanding the current boundaries in electronics. The integration of technologies like AI, machine learning, future communication systems (5G+, 6G), and the IoT requires innovations beyond the confines of computing, encompassing the entire spectrum of electronic systems and their applications. Emerging electronic devices, such as ReRAMs, CBRAMs, PCMs, MRAMs, FTJs, and FeFETs, are widely researched in this new era of technological innovation, due to their energy efficiency, compact size, and versatility, pushing the boundaries of what electronic circuits can achieve. Nevertheless, the path to fully realizing the potential of these device technologies is not without challenges. Issues such as scalability, manufacturing processes, reliability, and integration with conventional electronics present significant obstacles. Furthermore, the vast majority of the emerging devices researched to date are still a considerable distance away from being ready for large-scale commercialization, facing fundamental challenges in modeling, simulation, and circuit design. This special session aims to serve as a platform for the exchange of ideas and research findings in the field of emerging device technologies. It seeks to bring together researchers and experts in the field to discuss the latest developments, address the challenges, and explore the vast possibilities of these technologies. The goal is to foster collaboration and innovation, paving the way for the next generation of electronic circuits and systems that will shape the future of technology.

The topics of this special session include, but are not limited to:

- Physical and behavioral modeling of emerging device technologies
- Design of innovative adaptive analogue circuits
- Development of mem-computing arrays with emerging technologies
- Neural networks and neuromorphic circuits with emerging technologies
- CMOS integration of emerging technologies

**SS Organizers:** Ioannis Messaris, Technische Universität Dresden, DE  
Dimitrios Prousalis, Technische Universität Dresden, DE  
Ronald Tetzlaff, Technische Universität Dresden, DE

Wednesday, July 3<sup>rd</sup>, 16:00 – 17:00

Amphitheater 2

## Safety and Security in Modern System-on-Chip (SoC)

New challenges require new technologies, and new technologies pose new challenges. This is particularly evident in recent years concerning Cyber-Physical Systems (CPS). Will we be able to cope with the growing complexity of these devices that are increasingly interconnected and capable of acting and manipulating the surrounding reality? The enabling factor for CPS today is the possibility of creating pervasive and interconnected systems through the contribution of increasingly efficient Systems on Chip (SoCs), open-source Instruction Set Architecture (ISA), and AI accelerators. The risk management of these systems involves two orthogonal fields: i) Safety, in terms of hardware error resilience, and ii) Security, in terms of hardware/software solutions to reduce the attack surface of malicious actions. This special session proposes an in-depth exploration of the intricate relationship between the increasing performance of SoCs, the integration of AI, and the adoption of open-source architectures in both the Safety and Security domains. Through carefully examining these dimensions, our objective is to highlight and tackle the multifaceted challenges associated with ensuring the safety and security of next-generation computing systems.

The topics of this special session include, but are not limited to:

- Ensuring the robustness and reliability of AI algorithms in safety-critical applications
- Open-Source ISA Security
- Next-Gen SoCs: Performance and Complexity Challenges
- Secure Boot and Trusted Execution Environments
- Case Studies and Practical Solutions
- Techniques to enhance the dependability and fault tolerance of AI hardware accelerators

**SS Organizers:** Eleonora Vacca, Politecnico di Torino, IT  
Francesco Barchi, University of Bologna, IT

# EDA COMPETITION



Wednesday, July 3<sup>rd</sup>, 13:50 – 15:30

Amphitheater 1

Thursday, July 4<sup>th</sup>, 9:30 – 10:30

Amphitheater 1

## COMPETE FOR THE \$1000 AND JOIN THE HALL-OF-FAME

As usual in **SMACD Conferences**, the **2024 edition**, which will take place at Volos, Greece, from the 2nd to the 5th of July,, will also hold a thrilling and dynamic event where M.Sc. and Ph.D. students can compete with their best ideas, methodologies, flows and tools with one unique yet challenging goal:

## ENHANCE DESIGN AUTOMATION FOR INTEGRATED CIRCUITS AND SYSTEMS

The winner(s) of the event will receive a prize of **\$1,000** sponsored by



## HOW TO ENTER THE COMPETITION?

All participants must submit a paper (following the same SMACD 2024 submission guidelines) with a description of the methodology and/or tool, the design problem of their choice and the solution provided by their methodology and/or tool.

## EVALUATION CRITERIA

A Judging Committee will select the winner(s) based on the quality of the paper, of its presentation at the conference, and the live demonstration, using the following criteria:

- **Complexity** of the problem posed in the paper.
- **Level of automation** (e.g., fully automated, user-assisted, etc.).
- **Designer interface** (e.g., problem setup, result analysis, etc.).
- **Applicability of the proposal** (e.g., general approach or restricted to special problems, circuit classes or sizes, etc.).
- **Robustness** of the design solutions (e.g., against parasitics, variability, etc.) and, of the proposal itself (e.g. convergence, insensitivity to input and starting values, etc.).
- **Integration** degree with commercial design suites and design methodologies (e.g., import and export data from these suites, usability in one or more steps of current design flows, etc.).

## TOPICS OF INTEREST

Methodologies and tools related to all topics of the SMACD24 conference (e.g., Synthesis, Sizing, Optimization, Modeling and Simulation of AMS, RF and multidomain circuits, ML and Cloud Computing EDA methodologies, EDA methodologies for Hardware Security and Emerging Devices, etc.)

# IC DESIGN CONTEST



Friday, July 5<sup>th</sup>, 11:00 – 12:40

Amphitheater 2

## COMPETE FOR THE \$1000 AND JOIN THE HALL-OF-FAME

The **2024 edition** of the **SMACD Conference**, which will take place at Volos, Greece, from the 2nd to the 5th of July, will also hold a thrilling and dynamic event where M.Sc. and Ph.D. students can compete with their best use of EDA methodologies, to reach one unique yet challenging goal:

## ENHANCE INTEGRATED CIRCUITS AND SYSTEMS DESIGN

The winner(s) of the event will receive a prize of **\$1,000 (CHF800)** sponsored by



## HOW TO ENTER THE COMPETITION?

All participants must submit a paper (following SMACD 2024 submission guidelines) that fits into one or more of the following categories:

- Novel IC designs whose performances compete within the state-of-the-art of its research field (at least including Post-Layout simulations);
- IC designs where at least one step of its development flow was partially (or fully) assisted by custom/academic Computer-Aided Design and/or Electronic Design Automation tools;
- IC designs clearly identifying one or more steps of the development flow that would greatly benefit from the development of new Computer-Aided Design and/or Electronic Design Automation tools.

## EVALUATION CRITERIA

A Judging Committee will select the winner(s) based on the quality of the paper, of its presentation at the conference, and the live demonstration, using the following criteria:

- **Complexity** of the problem posed in the paper.
- **Level of EDA support** to reach the presented IC design.
- **Robustness** of the design solutions (e.g., against parasitics, variability, etc.).

## TOPICS OF INTEREST

IC designs resulting or enhanced by EDA methodologies and tools related to all application topics of the SMACD24, e.g., AMS, RF and multidomain circuits, and, also, emerging devices.

# TECHNICAL PROGRAM



Tuesday, July 2<sup>nd</sup>

09:00 - 10:30

Amphitheater 1

**Tutorial: "Machine Learning for Design Automation"**

11:00 - 12:30

Amphitheater 1

**Tutorial: "Tackling Signal Integrity Challenges in Interposer and 3DIC Applications with Ansys RaptorX"**

13:30 - 15:00

Amphitheater 1

**Tutorial: "Exploring Radiation Effects for Reconfigurable SoCs in Space and Particle Accelerators"**

15:30 - 17:00

Amphitheater 1

**Tutorial: "Integrating Multiple Knowledge-based Automation Methodologies into the A/MS IC Design Flow"**

# Wednesday, July 3<sup>rd</sup>

8:30 - 9:00

Amphitheater 1

## Opening Ceremony

9:00 - 10:00

Amphitheater 1

## Plenary Talk: *Prof. Yusuf Leblebici*, "Designing Some of the Most Influential Hardware in Human History: Our Collective Responsibilities"

Chair: Alkis Hatzopoulos

1A

10:30 - 12:10

Amphitheater 1

## Automated Circuit Design

Chairs: Helmut Graeb, Francisco Fernandez

### 10:30 Solving the Inverse Problem of Analog Integrated Circuit Sizing with Diffusion Models

Pedro Eid (Instituto de Telecomunicações / Instituto Superior Técnico)

Filipe Azevedo (Instituto de Telecomunicações / Instituto Superior Técnico)

Ricardo Martins (Instituto de Telecomunicações / Instituto Superior Técnico)

Nuno Lourenço (Instituto de Telecomunicações / Instituto Superior Técnico)

### 10:50 A CAD Toolbox for the Automatic Design and Optimization of ULP CMOS Voltage References

Andrea Boni (University of Parma, Dept. of Engineering and Architecture)

Michele Caselli (University of Parma, Dept. of Engineering and Architecture)

### 11:10 Advanced Analog Design Optimization: Comparison Between Reinforcement Learning and Heuristic Algorithms

Michel Chevalier (STMICROELECTRONICS)

Severin Trochut (STMicroelectronics)

Roberto Guizzetti (STMicroelectronics)

Pascal Urard (STMicroelectronics)

Lioua Labrak (Institut des Nanotechnologies de Lyon)

Rémy Cellier (Institut des Nanotechnologies de Lyon)

John Samuel (LIRIS)

Nacer Abouchi (Institut des Nanotechnologies de Lyon)

### 11:30 A novel simulations scheduler for automated circuit sizing algorithms

Catalin Visan (University "Politehnica" of Bucharest)

Dan Curavale (University "Politehnica" of Bucharest)

Georgian Nicolae (University "Politehnica" of Bucharest)

Mihai Boldeanu (University "Politehnica" of Bucharest)

Horia Cucu (University "Politehnica" of Bucharest)

Andi Buzo (Infineon Technologies)

### 11:50 Algorithm-based Wide-Band Impedance Matching Network Synthesis and Optimization

Anastasios Michailidis (Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki)

Thomas Noulis (Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki)

**1B** **10:30 - 12:10** **Amphitheater 2**  
**Special Session: "Advances & Future Trends in Electronic Circuits & Systems with Emerging Devices"**  
**Chairs: Ioannis Messaris, Dimitrios Prousalis**

**10:30 An Efficient FeFET-Based Compute-In-Memory Macro Readout Inspired by the 3T Pixel Array Cell**

Nellie Laleni (*Fraunhofer IPMS*)  
Thomas Kämpfe (*Fraunhofer IPMS*)

**10:50 Circuit Component Tolerance of Self-Organizing Logic Gates**

Haik Manukian (*Naval Information Warfare Center Pacific*)  
Osama Nayfeh (*Naval Information Warfare Center Pacific*)  
Matthew Kelly (*Naval Information Warfare Center Pacific*)

**11:10 Image Processing with Memristor Cellular Nonlinear Networks Featuring Volatile Threshold Switches**

Dimitrios Prousalis (*Technische Universität Dresden - TU Dresden*)  
Ioannis Messaris (*Technische Universität Dresden*)  
Ahmed Ali Sayed (*Technische Universität Dresden*)  
Vasileios Ntinis (*Faculty of Electrical and Computer Engineering, Technische Universität Dresden*)  
Ahmet Samil Demirkol (*IEE-GE, Technical University of Dresden*)  
Alon Ascoli (*Department of Electronics and Telecommunications, Politecnico di Torino*)  
Ronald Tetzlaff (*TU Dresden*)

**11:30 An Optimization Framework for Mixed-Signal Accelerators Based on F-2T2R Compute Cells**

Michele Caselli (*University of Parma*)  
Andrea Boni (*University of Parma*)

**11:50 FPGA Implementation of an Elementary ReRAM Memory Control Unit**

Patricio Carrasco (*Universidad Tecnica Federico Santa Maria*)  
Ioannis Vourkas (*Universidad Tecnica Federico Santa Maria*)

**13:20 - 13:50**  
**CEDA Presentation**

**Amphitheater 1**

**2A** **13:50 - 15:30** **Amphitheater 1**  
**EDA Competition I**  
**Chairs: Elisenda Roca, Vasilis Pavlidis**

**13:50 Presentation EDA Competition**

**14:00 Procedural Design, Verification and Implementation Framework for Analog Amplifiers**

Veeti Lahtinen (*Department of Electronics and Nanoengineering, Aalto University*)  
Santeri Porrasmaa (*Department of Electronics and Nanoengineering, Aalto University*)  
Marko Kosunen (*Department of Electronics and Nanoengineering, Aalto University*)  
Jussi Rynnänen (*Department of Electronics and Nanoengineering, Aalto University*)

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**14:30 Automatic Regression Framework for MRAM Compact Models Calibration including Stochasticity**

Pierre Graindorge (*imec, University of Liege*)

Bowen Wang (*imec*)

Marie Garcia Bardon (*imec*)

Fernando Garcia Redondo (*imec*)

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**15:00 Area-Aware Logic Mapping for MAGIC based In-Memory Computing**

Jiaxiang Pan (*Ningbo University*)

Zhufei Chu (*Ningbo University*)

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**2B 13:50 - 15:30 Amphitheater 2**  
**Cutting-edge Technologies for Automotive and Space**  
**Chair: TBD**

**13:50 Bidirectional CAN-Interface Using Inductive Transmission**

Arne von Zedlitz-Neukirch (*Chair of High Frequency Electronics, RWTH Aachen University*)

David Bierbüsse (*Chair of High Frequency Electronics, RWTH Aachen University*)

Renato Negra (*Chair of High Frequency Electronics, RWTH Aachen University*)

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**14:10 Design and Development of a Linear Adaptive Equalizer used for High Data-Rate Satellite Receivers based on CCSDS 131.2-B Standard**

Nico Corsinovi (*University of Pisa*)

Emanuele Pagani (*IngeniArs S.r.l., University of Pisa*)

Roberto Ciardi (*IngeniArs S.r.l., University of Pisa*)

Matteo Bertolucci (*IngeniArs S.r.l.*)

Luca Fanucci (*University of Pisa*)

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**14:30 Battery Temperature Prediction in Electric Vehicles Using Bayesian Regularization**

Rusen Alp Akpınar (*Cranfield University, Faraday Institution and Advanced Propulsion Centre (APC)*)

Abbas Fotouhi (*Cranfield University, Faraday Institution and Advanced Propulsion Centre (APC)*)

Hanwen Zhang (*Cranfield University*)

Daniel Auger (*Cranfield University*)

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**14:50 The Integration and Testing Procedures for the AcubeSAT Nanosatellite's Software**

Antonios Keremidis (*Aristotle University of Thessaloniki*)

Stylios Tzelepis (*National Technical University of Athens*)

Alkis Hatzopoulos (*Electronics Lab, Dept. of Electrical and Computer Eng., Aristotle University of Thessaloniki*)

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**15:10 Photo Diode Amplifier Design for Radiation Signal Processing with Applications in Mössbauer Spectroscopy for Space Exploration**

Mohammad Beyki (*Leibniz University Hannover, Hochschule Hannover - University of Applied Sciences and Arts*)

Justus Pawlak (*Leibniz University Hannover, Hochschule Hannover - University of Applied Sciences and Arts*)

Robert Patzke (*Hochschule Hannover - University of Applied Sciences and Arts*)

Franz Renz (*Institute of Inorganic Chemistry, Leibniz University, Hannover, D-30167, Germany*)

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3A

16:00 - 17:00

Amphitheater 1

## Innovations in Hardware Security I

Chair: Giulia di Capua

**16:00 Harvesting RTN for True Random Number Generators and Physical Unclonable Functions**Francisco J. Rubio Barbero (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Fernando de Los Santos Prieto (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Rafael Castro Lopez (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Elisenda Roca Moreno (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)Francisco V. Fernandez Fernandez (*Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla)*)**16:20 Proposal and Implementation on Smartphone of a PUF Using Accelerometers and Gyroscopes**Raúl Aparicio-Téllez (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Miguel Garcia-Bosque (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Guillermo Díez-Senorans (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Abel Naya (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)Santiago Celma (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)**16:40 Sensitivity-aware Hardware Trojan Injection for SET Propagation and Soft Error Attacks**Alexandra Takou (*University of Thessaly*)Georgios-Ioannis Paliaroutis (*University of Thessaly*)Pelopidas Tsoumanis (*University of Thessaly*)George Stamoulis (*University of Thessaly*)Nestor Evmorfopoulos (*University of Thessaly*)

3B

16:00 - 17:00

Amphitheater 2

## Machine Learning for Modeling

Chair: Alex Doboli

**16:00 Neural Network-Based Coefficient Estimators for Memory Polynomial Digital Predistortion**Elif Seher Serinken (*Yildiz Technical University Electronics and Communications Engineering Department*)Alperen Tunç (*Istanbul Technical University Electronics and Communications Engineering Department*)Revna Acar-Vural (*Yildiz Technical University Electronics and Communications Engineering Department*)Mustafa Berke Yelten (*Istanbul Technical University Electronics and Communications*)**16:20 Low-Power 9.6-11GHz and 10.8-12GHz VCOs Designed for a 2.5/5GHz TRx using High-Q Inductors Synthesized with ML Techniques**Fabio Passos (*Instituto de Telecomunicações*)Nuno Lourenço (*Instituto de Telecomunicações*)Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon*)**16:40 An Open-Source ANN-based Analog/RF Intellectual Property for SkyWater130nm Technology**Enes Sağlıcan (*Gebze Technical University*)Engin Afacan (*Gebze Technical University*)

# Thursday, July 4th

8:30 - 9:30

Amphitheater 1

## Plenary Talk: *Prof. Georges Gielen*, "Designing Analog Integrated Circuits: Designers, Synthesis or Generative AI?"

Chair: Francisco Fernandez

4A

9:30 - 10:30

Amphitheater 1

EDA Competition II

Chairs: Elisenda Roca, Vasilis Pavlidis

### 9:30 Multiple Output Modelling of Integrated Circuits Behavior Using an Active Learning Approach

Vasile Grosu (*"Gheorghe Asachi" Technical University of Iasi*)

David Emilian (*Infineon Technologies*)

Liviu Goras (*"Gheorghe Asachi" Technical University Iasi*)

Georg Pelz (*Infineon Technologies AG Neubiberg*)

### 10:00 Fast ML-driven Analog Circuit Layout using Reinforcement Learning and Steiner Trees

Davide Basso (*University of Trieste*)

Luca Bortolussi (*University of Trieste*)

Mirjana Videnovic-Misic (*Infineon Technologies Austria*)

Husni Habal (*Infineon*)

11:00 - 12:00

Amphitheater 1

## Sponsor Presentations

5A

13:40 - 15:00

Amphitheater 1

Automating Layout and Technology Migration

Chair: Jürgen Scheible

### 13:40 Effective Routing Probability Maps via Convolutional Neural Networks for Analog IC Layout Automation

Diogo Penada (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

Nuno Lourenço (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

Nuno Horta (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

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**14:00 Mitigating Power and Process Variation for Analog CIM Design Migration**

Shih-Han Chang (*National Yang Ming Chiao Tung University*)  
Shih-Yu Chen (*National Yang Ming Chiao Tung University*)  
Chun-Wen Yang (*National Yang Ming Chiao Tung University*)  
Hau-Wei Huang (*National Yang Ming Chiao Tung University*)  
Yu-Cheng Yang (*National Yang Ming Chiao Tung University*)  
Wei-Liang Chen (*National Yang Ming Chiao Tung University*)  
Chien-Nan Liu (*National Yang Ming Chiao Tung University*)  
Hung-Ming Chen (*National Yang Ming Chiao Tung University*)

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**14:20 Ternary Clock Tree Synthesis for 3D ICs**

Christos Pavlidis (*Aristotle University of Thessaloniki*)  
Nikos Sketopoulos (*University of Thessaly*)  
Christos Sotiriou (*University of Thessaly*)  
Vasilis Pavlidis (*Aristotle University of Thessaloniki*)

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**14:40 PONDEROUS: A Performance-driven Analog IC Placement Optimizer Leveraged by a ML Pipeline**

Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)  
António Gusmão (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)  
Rafael Vieira (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)  
Fábio Passos (*Instituto de Telecomunicações, Portugal*)  
Nuno Lourenço (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)  
Nuno Horta (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisboa*)

**5B****13:40 - 15:00****Amphitheater 2****Advanced Circuit Design I****Chair: Ioannis Vourkas****13:40 Carry-chain based Ring Oscillator Design for Temperature Sensing on FPGAs**

Fanny Spagnolo (*University of Calabria - DIMES*)  
Pasquale Corsonello (*University of Calabria - DIMES*)

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**14:00 A Hardware Efficient Digital DAC Linearization Topology for Delta-Sigma ADCs**

Jesko Flemming (*Institute for Sensors and Automation, University of Applied Sciences and Arts Hannover, Germany*)  
Timon Rogge (*Institute for Sensors and Automation, University of Applied Sciences and Arts Hannover, Germany*)  
Bernhard Wicht (*Institute of Microelectronic Systems, Leibniz University Hannover*)  
Pascal Witte (*Institute for Sensors and Automation, University of Applied Sciences and Arts Hannover, Germany*)

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**14:20 A PWM-SAR ADC with Asynchronous Control Unit for Mixed-Signal Accelerators**

Michele Caselli (*University of Parma*)  
Andrea Boni (*University of Parma*)  
Stefano Caselli (*University of Parma*)

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**14:40 3.35V High Voltage Electroforming Generator in 28nm with 5.3mV ripple and 46% efficiency for HfO<sub>2</sub> based Memristors**

Muhammad Shamookh (*Forschungszentrum Jülich-ZEA-2, IIC Technische Universität Hamburg*)  
Arun Ashok (*Forschungszentrum Jülich-ZEA-2*)  
Andre Zambanini (*Forschungszentrum Jülich-ZEA-2*)

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6A

15:30 - 16:30

Amphitheater 1

## EDA and the Human Factor

Chair: Engin Afacan

**15:30 Streamlined design methodology for Cell-Based DCOs**Andres Santana-Andreo (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)J.M. Gata-Romero (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)Rafael Castro-Lopez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)Elisenda Roca (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)Francisco Vidal Fernandez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)**15:50 Design of a Two-Stage Miller-Compensated Operational Amplifier Using a Designer-in-the-Loop EDA Approach**Yijia Hao (*University of Glasgow*)Miguel Gandara (*Mediatek Inc.*)Srinjoy Mitra (*University of Edinburgh*)Sandy Cochran (*University of Glasgow*)Bo Liu (*University of Glasgow*)**16:10 Automatically Understanding Human Behavior for IoT Applications with Optimized Human-in-the-Loop Control**Himavanth Reddy Pallapu (*Stony Brook University, Department of ECE*)Gnaneswar Villuri (*Stony Brook University, Department of ECE*)Simona Doboli (*Department of Computer Science*)Alex Doboli (*Stony Brook University, Department of ECE*)

6B

15:30 - 16:30

Amphitheater 2

## Special Session: "Safety and Security in System-on-Chip (SoC)"

Chair: Eleonora Vacca

**15:30 OP-TEE powered OpenSSL Engine enhancing Digital Signature security for ARM Architectures**Franco Volante (*Politecnico di Torino*)Francesco Barchi (*Università di Bologna*)Edoardo Patti (*Politecnico di Torino*)Lorenzo Bottaccioli (*Politecnico di Torino*)Luca Barbierato (*Politecnico di Torino*)**15:50 Exploring the Resiliency of Hardware CNN for Aerospace Application**Corrado De Sio (*Politecnico di Torino*)Giorgio Cora (*Politecnico di Torino*)Sarah Azimi (*Politecnico di Torino*)Eleonora Vacca (*Politecnico di Torino*)Luca Sterpone (*Politecnico di Torino*)**16:10 End-to-end Integration of OpenTitan Security Features in a Pure RISC-V SoC**Alberto Musa (*Università di Bologna*)Emanuele Parisi (*Università di Bologna*)Luca Barbierato (*Politecnico di Torino*)Andrea Acquaviva (*Università di Bologna*)Francesco Barchi (*Università di Bologna*)

# Friday, July 5<sup>th</sup>

7A

9:30 - 10:30

Amphitheater 1

Novel Device Modeling and Characterization

Chair: *TBD*

**9:30 Method, Testing Procedure and System for the Experimental Characterization of Power Inductors**

Giulia Di Capua (University of Cassino and Southern Lazio)  
Nicola Femia (DIEM - University of Salerno)  
Nunzio Oliva (Exeling Srl)  
Luca De Guglielmo (Exeling Srl)

**9:50 A Verilog-A/MS Compact Model for the Temperature Dependency of the Open-Circuit Voltage for Integrated Diodes**

Pablo Fernández-Peramo (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)  
Juan Antonio Leñero-Bardallo (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)  
Sergio Palomeque-Mangut (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)  
Ángel Rodríguez-Vázquez (*Instituto de Microelectrónica de Sevilla (IMSE-CNM) CSIC-Universidad de Sevilla*)

**10:10 Towards a Digital Twin of a Time-Dependent Variability Characterization Laboratory**

J.M. Gata-Romero (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)  
E. Roca (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)  
R. Castro-Lopez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)  
F.V. Fernandez (*Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla – CSIC, Seville, Spain*)

7B

9:30 - 10:30

Amphitheater 2

Advanced circuit design II

Chair: *Michele Caselli*

**9:30 A New Metric Measuring Steering Accuracy of Digitally Controlled Phase Shifters**

Francisco Aznar (*Centro Universitario de la Defensa Zaragoza*)  
Uxua Esteban-Eraso (*Universidad de Zaragoza*)  
Antonio Dionisio Martínez-Pérez (*Universidad de Zaragoza*)  
Santiago Celma (*Universidad de Zaragoza*)

**9:50 A 25 nW Heartbeat Monitoring Circuit for Wearable Applications in CMOS 65nm**

Rafael Vieira (*Instituto de Telecomunicações*)  
Seyedehsomayeh Hatefinasab (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon*)  
Ricardo Martins (*Instituto de Telecomunicações, Instituto Superior Técnico – ULisbon*)  
Nuno Horta (*Instituto de Telecomunicações*)

**10:10 Low-Power Encoding for PAM-3 DRAM Bus**

Jonghyeon Nam (*Hanyang University*)  
Jaeduk Han (*Hanyang University*)  
Hokeun Kim (*Arizona State University*)

8A

11:00 - 12:40

Amphitheater 1

Machine Learning for Design

Chair: TBD

**11:00 A learning-based method for performance optimization of timing analysis**

Anastasis Vagenas (*University of Thessaly*)  
Dimitrios Garyfallou (*University of Thessaly*)  
Nestor Evmorfopoulos (*University of Thessaly*)  
George Stamoulis (*University of Thessaly*)

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**11:20 Optimizer-Free Sizing of OpAmps Leveraging Structural and Functional Properties**

Markus Leibl (*Technical University of Munich (TUM)*)  
Helmut Graeb (*Technical University of Munich (TUM)*)

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**11:40 Frontend-Backend Integrated Circuit Device Linking Using Machine Learning Algorithms**

Ingrid Kovacs (*Technical University of Cluj-Napoca*)  
Bianca Carbunescu-Stoenescu (*Technical University of Cluj-Napoca*)  
Andi Buzo (*Infineon Technologies AG Neubiberg*)  
Emilian David (*Infineon Technologies Bucharest*)  
Georg Pelz (*Infineon Technologies AG Neubiberg*)  
Marina Topa (*Technical University of Cluj-Napoca*)

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**12:00 ANN-based Analog/RF IC Synthesis Featuring Reinforcement Learning-based Fine-Tuning**

Hakan Taşkıran (*Gebze Technical University*)  
Enes Sağlıcan (*Gebze Technical University*)  
Engin Afacan (*Gebze Technical University*)

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**12:20 Analog Circuit Classification Using Graph Convolution Networks**

Husni Habal (*Infineon Technologies AG*)  
Marco De Maina (*Infineon Technologies AG*)  
Vishnu Pathak (*Infineon Technologies India Pvt. Ltd.*)  
Karthik Salian (*Infineon Technologies India Pvt. Ltd.*)

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8B

11:00 - 12:40

Amphitheater 2

IC Design Contest

Chairs: Georgios Panagopoulos, Dimitrios Garyfallou

**11:00 Set the Clock: A Synthesizable Clock Manager**

Jonas Lienke (*Insitut für Mikroelektronik und Mechatronik Systeme gemeinnützige GmbH*)  
Florian Kögler (*IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH*)  
Eric Schäfer (*IMMS GmbH*)  
Georg Gläser (*Insitut für Mikroelektronik und Mechatronik Systeme gemeinnützige GmbH*)

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**11:25 Two Stage Diode-String Architecture for Ultra-Low Power Digital to Analog Converters**

Andreas Tsioungkos (*Aristotle University of Thessaloniki*)  
Moschos Antoniadis (*Aristotle University of Thessaloniki*)  
Vasilis Pavlidis (*Aristotle University of Thessaloniki*)

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**11:50 Rapid Prototyping Platform for Integrated Circuits for Quantum Computing**

Jonas Mair (ZEA-2)

Sabitha Kusuma (ZEA-2)

Daniel Liebau (ZEA-2)

Lammert Duipmans (ZEA-2)

Patrick Vliex (ZEA-2)

André Zambanini (ZEA-2)

Stefan van Waasen (ZEA-2, *Uni DUE*)

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**12:15 DTCO for Fast STT-MRAM Periphery Operation**

Ahmed Hossam-Eldeen (IMEC, Leuven, Belgium / University of Gent, Gent, Belgium)

Bowen Wang (IMEC, Leuven, Belgium), Priyanka Pandey (IMEC, Leuven, Belgium)

Marie Garcia Bardon (IMEC, Leuven, Belgium)

Fernando Garcia Redondo (IMEC, Leuven, Belgium)

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**9A****13:50 - 14:50****Amphitheater 1****Advanced Circuit Modeling****Chair: Nicola Femia****13:50 Efficient Parametric Model Order Reduction for Large-Scale Circuit Models using Extended Krylov Subspace**

Chrysostomos Chatzigeorgiou (University of Thessaly)

George Floros (University of Thessaly)

Dimitrios Chatzigeorgiou (University of Thessaly)

Nestor Evmorfopoulos (University of Thessaly)

George Stamoulis (University of Thessaly)

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**14:10 Propagation Delay Estimation for Mixed-Signal Modeling of Comparators**

Martin Grabmann (IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH))

Eric Schäfer (IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH))

Georg Gläser (IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH))

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**14:30 Analysis and Simulation of Reset Leakage Currents and Quantization Error in a PFM Digital Pixel**

Sergio Palomeque-Mangut (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

Pablo Fernández-Peramo (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

Juan Antonio Leñero-Bardallo (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

Ángel Rodríguez-Vázquez (Institute of Microelectronics of Seville (IMSE-CNM), CSIC-Universidad de Sevilla, Spain)

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**9B****13:50 - 14:50****Amphitheater 2****Innovations in Hardware Security II****Chair: Ricardo Martins****13:50 Optimization-based bit selection technique to improve the reliability of PUFs**

Fernando de Los Santos Prieto (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Francisco Javier Rubio Barbero (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Rafael Castro López (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Elisenda Roca Moreno (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

Francisco V. Fernández Fernández (Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla))

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**14:10 Towards the Implementation of a Strong PUF using Generalized Galois Ring Oscillators**

Raúl Aparicio-Téllez (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

Miguel Garcia-Bosque (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

Guillermo Diez-Senorans (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

Santiago Celma (*Group of Electronic Design (GDE), I3A, University of Zaragoza*)

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**14:30 A Fast Security Closure Approach for EM-based Attacks on General Multi-Segment Interconnects**

Pavlos Stoikos (*University of Thessaly*)

George Floros (*University of Thessaly*)

Nestor Evmorfopoulos (*University of Thessaly*)

George Stamoulis (*University of Thessaly*)

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10A

15:20 - 16:20

Amphitheater 1

Dealing with Reliability

Chair: Alkiviadis Hatzopoulos

**15:20 Stress-based Electromigration Modeling in IC Design: Moving from Theory to Practice**

Susann Rothe (*Dresden University of Technology*)

Jens Lienig (*Dresden University of Technology*)

Sachin S. Patnekar (*University of Minnesota*)

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**15:40 An Efficient Approach for Combined Electromigration and Thermomigration Analysis Based on the Extended Krylov Subspace**

Eleni Tselepi (*University of Thessaly*)

Olympia Axelou (*University of Thessaly*)

George Floros (*University of Thessaly*)

George Stamoulis (*University of Thessaly*)

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**16:00 Analysis of Capacitive Coupling and Crosstalk in the PCB of Switch-Mode Power Supplies**

Giulia Di Capua (*University of Cassino and Southern Lazio*)

Antonio Maffucci (*University of Cassino and Southern Lazio*)

Nicola Femia (*University of Salerno*)

Andrea Gaetano Chiariello (*Università degli Studi della Campania "Luigi Vanvitelli"*)

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10B

15:20 - 16:20

Amphitheater 2

Dealing with Verification

Chair: Miguel Garcia Bosque

**15:20 Efficient Stimuli Generation using Reinforcement Learning in Design Verification**

Deepak Narayan Gadde (*Infineon Technologies Dresden GmbH & Co. KG*)

Thomas Nalapat (*Infineon Technologies Dresden GmbH & Co. KG*)

Aman Kumar (*Infineon Technologies Dresden GmbH & Co. KG*)

Sebastian Simon (*Infineon Technologies Dresden GmbH & Co. KG*)

Djones Lettnin (*Infineon Technologies AG*)

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**15:40 Formal Verification of Nonlinear Analog Circuits using State Space-Based Model Order Reduction**

Yasmine Abu-Haeyeh (*University of Frankfurt*)

Lars Hedrich (*University of Frankfurt*)

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**16:00 Low-rank balanced truncation of RLCK models via frequency-aware rational Krylov-based projection**

Christos Giamouzis (*University of Thessaly*)

Dimitrios Garyfallou (*University of Thessaly*)

Nestor Evmorfopoulos (*University of Thessaly*)

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16:20 - 16:50

Amphitheater 1

**Award Ceremony and Closing**